**BSC ELECTRICAL AND ELECTRONICS ENGINEERING**

**TABLE OF CONTENTS.**

**1.BACKGROUND**………………………………………………………………………….….…..…3

1.1 Introduction…………………………………………………………………………..……….….3

1.2 Theory…...…………………………………………………………………………………………3

1.3 Objectives………………………………………………….………………………………....……4

1.4 Apparatus………………………………………………………………………………………….4

1.5 Circuit diagram…………………………………………………………………………………...4

1.6 Expected theoretical results……….……………………………………………………………6

**2 MATHEMATICAL MODEL**…………...…………………………………………………………..7

2.1 Model equations ……………………………………………………………………………….….7

2.2 Assumptions made…………………………………………………………………………..…….8

2.3 Experiment procedure……………………………………………………………………….……8

3. PRACTICAL IMPLEMENTATION……………………………………………………….……..9

3.1 Set up of the circuit in prototyping ………………..…………………………………………..10

3.2 Data and measurements…………………………………………………………………….…..10

**4 RESULTS**……………………………………………………………………………….……………10

**5 DISCUSSION CONCLUSION & RECOMMENDATION**………………………….…………11

**Figure 1** layout diagram of adder circuit using op amp………………………..……………......4

**Figure 2** layout diagram of subtractor circuit using op amp……..……………………………..5

**Figure 3** Circuit diagram of adder and subtractor circuits using op amp………………….…9

**Figure 4** Table of result for adder circuit……………………………………….…..….……….…10

**Figure 5** The table of result for subtractor circuit………………………………………..………10

**Figure 6** The output of the adder circuit using op amp………………………………………….10

**Figure 7** The output of the subtractor circuit using op amp……………………..…………..…11

**1BACKGROUND**

**1.1 Introduction for adder**

Fine-Tuning Frequency Response: The objective is to achieve a precisely optimized frequency response for the differentiator circuit utilizing an inverting operational amplifier IC 741.

Benefits: A meticulously adjusted frequency response ensures that the circuit adeptly distinguishes signals within the desired frequency range. This is particularly critical for applications where specific frequency components need accentuation or filtration. Achieving an optimal response elevates the circuit's effectiveness in signal processing tasks.

Minimizing Noise and Improving Stability: The aim is to employ strategies that reduce noise and enhance the stability of the differentiator circuit using an inverting op-amp IC 741.

Benefits: Noise can present a significant challenge in high-frequency circuits. By concentrating on noise reduction techniques, such as incorporating low-pass filters or employing shielding methods, the circuit's vulnerability to undesired signals can be minimized. Enhancing stability ensures the circuit operates reliably across diverse conditions, contributing to its resilience in real-world applications.

**Introduction for subtractor**

The Subtractor Circuit, stemming from the Summing Amplifier, assumes a crucial role in applications necessitating the subtraction operation. Leveraging the versatile traits of operational amplifiers, particularly the widely employed IC 741, the Subtractor Circuit enables meticulous and precise subtraction by deducting one input signal from another.

Essentially, the Subtractor Circuit utilizes operational amplifiers to perform the subtraction operation by adjusting the weights of input signals. This configuration proves particularly advantageous in scenarios demanding the calculation of the difference between two analog voltages with a high level of accuracy.

**1.2 Theory**

**For adder:**

The Adder Circuit, also known as the Summing Amplifier, employs an operational amplifier to combine multiple input signals into a single output voltage. The fundamental principle aims to achieve an output voltage representing the algebraic sum of the weighted input voltages, with the IC 741 operational amplifier serving as the central amplifying component.

Configuration:

The basic arrangement of the Adder Circuit includes an inverting operational amplifier with multiple input resistors (R1, R2, ..., Rn) connected to the inverting terminal. Each input signal (V1, V2, ..., Vn) is introduced through its respective input resistor, and a feedback resistor (Rf) connects from the inverting terminal to the output.

For the Subtractor Circuit:

As a specialized version of the Summing Amplifier, the Subtractor Circuit utilizes an operational amplifier to perform the subtraction operation between two input voltages with precision. In this design, the circuit is specifically tailored to compute the exact difference between the input voltages, with the operational amplifier, typically the IC 741, playing a crucial role in ensuring accurate amplification and subtraction.

Configuration:

The basic layout of the Subtractor Circuit involves an inverting operational amplifier with two input resistors (R1 and R2). The inverting terminal is connected to both input signals, and a feedback resistor (Rf) links from the inverting terminal to the output.

**1.3 objectives**

* Study the applications of IC 741 as adder and subtractor

**1.4 Apparatus**

1.IC 741.

2. Resistors (1 kΩ) --- 4.

3. Transistor regulated power supply (TPS).

4. IC bread board trainer.

5. Cathode ray oscilloscope.

6. Signal generator (function generator)

**1.5 Circuit diagrams**

**adder circuit**



***figure 1 layout diagram of odder (summing amplifier) circuit using op amp IC 741***

**subtractor circuit**



***figure 2 layout diagram of subtractor circuit using op amp IC 741***

**Critical Components for Adder Circuit**

1. Operational Amplifier:

The operational amplifier magnifies the voltage difference between its inverting and non-inverting inputs. The IC 741 is frequently chosen for its reliability and widespread availability.

2**. Input Resistors (R1, R2, ..., Rn):**

Each input signal corresponds to an input resistor, dictating the significance of that specific input in the summation process. The larger the resistor, the lesser the significance.

3. Feedback Resistor (Rf):

The feedback resistor sets the overall gain of the circuit and establishes the scaling factor for the combined input signals.

**Essential Elements for Subtractor Circuit**

1. **Operational Amplifier**:

The operational amplifier amplifies the voltage difference between its inverting and non-inverting inputs. The IC 741 is commonly selected for its reliability and wide availability.

2. **Input Resistors (R1 and R2):**

Two input resistors are linked to the two input signals (V1 and V2). The voltage difference at the inverting terminal is determined by the weighted distinction of the input voltages.

3. Feedback Resistor (Rf):

The feedback resistor sets the overall gain of the circuit and determines the scaling factor for the subtracted input signals.

**1.6 Expected theoretical results**

**Adder:**

1. Voltage Accumulation:

The Adder Circuit is engineered to accumulate multiple input voltages, resulting in the output voltage (Vout) representing the algebraic sum of the weighted input voltages. Mathematically, this can be expressed as: Vout=−(R1Rf⋅V1+R2Rf⋅V2+…+RnRf⋅Vn)

2. Weighted Accumulation:

The output voltage is a linear combination of the input voltages, with weights determined by the ratios of the feedback resistor (Rf) to the respective input resistors (R1, R2, ..., Rn).

3. Adjustable Amplification:

The overall gain of the circuit can be tailored by adjusting the values of the feedback resistor (Rf) and the input resistors (R1, R2, ..., Rn). This allows for control over the amplification of the combined input signals.

Subtractor:

1. Voltage Deduction:

The Subtractor Circuit is designed to compute the difference between two input voltages, resulting in the output voltage (Vout) representing the amplified difference between the two input voltages. Mathematically, this can be expressed as: Vout=−(R1Rf⋅V1−R2Rf⋅V2)

2. Difference Amplification:

The output voltage is a linear combination of the difference between the input voltages, with the weights determined by the ratios of the feedback resistor (Rf) to the input resistors (R1 and R2).

3. Adjustable Amplification:

Similar to the Adder Circuit, the overall gain of the Subtractor Circuit can be adjusted by varying the values of the feedback resistor (Rf) and the input resistors (R1 and R2). This provides control over the amplification of the difference between the input signals.

**2. MATHEMATICAL MODEL**

**2.1 Model equations**

**For adder**

The output voltage (*V*out​) for the Adder Circuit is given by the weighted sum of the input voltages:

*V*out​=−(*R*1​*Rf*​​⋅*V*1​+*R*2​*Rf*​​⋅*V*2​+…+*Rn*​*Rf*​​⋅*Vn*​)

This equation represents the linear combination of the input voltages (*V*1​,*V*2​,...,*Vn*​) with weights determined by the ratios of the feedback resistor (*Rf*​) to the corresponding input resistors (*R*1​,*R*2​,...,*Rn*​). The negative sign indicates the inversion of the output with respect to the input summation.

**For the subtractor**

The output voltage (*V*out​) for the Subtractor Circuit is given by the amplified difference between two input voltages:

*V*out​=−(*R*1​*Rf*​​⋅*V*1​−*R*2​*Rf*​​⋅*V*2​)

Similar to the Adder Circuit, this equation represents the linear combination of the difference between two input voltages (*V*1​ and *V*2​), with weights determined by the ratios of the feedback resistor (*Rf*​) to the input resistors (*R*1​ and *R*2​). The negative sign indicates the inversion of the output with respect to the input difference.

**2.2 Assumptions made**

**For the adder:**

1. Ideal Operational Amplifier (Op-Amp):

The operational amplifier is presumed to be ideal, possessing infinite open-loop gain, infinite input impedance, zero output impedance, and no offset voltage. While real Op-Amps have limitations, assuming ideality simplifies the analysis.

2. Negligible Input Bias Current:

The input bias current of the operational amplifier is considered negligible. Although real Op-Amps exhibit some input bias current, for analytical purposes, it is deemed small enough not to significantly impact the circuit.

3. Zero Input Offset Voltage:

The input offset voltage of the operational amplifier is assumed to be zero. In practical terms, Op-Amps may have slight offset voltages, but this assumption streamlines the model.

4. Ideal Resistors: Resistors within the circuit are treated as ideal, devoid of parasitic effects, temperature dependence, or manufacturing tolerances. While this simplifies calculations, it may not accurately represent real-world resistor characteristics.

5. Linear Operation:

The circuit is expected to function in the linear region of the operational amplifier, where the output is directly proportional to the input. Non-linear effects are disregarded.

**For the subtractor**:

1. Ideal Operational Amplifier (Op-Amp):

Similar to the Adder Circuit, the operational amplifier in the Subtractor Circuit is assumed to be ideal, simplifying the analysis.

2. Negligible Input Bias Current:

As in the Adder Circuit, the input bias current of the operational amplifier is considered negligible.

3. Zero Input Offset Voltage:

The assumption of zero input offset voltage for the operational amplifier is retained in the Subtractor Circuit.

4. Ideal Resistors:

Resistors within the circuit are presumed to be ideal, lacking parasitic effects, temperature dependence, or manufacturing tolerances.

5. Linear Operation:

The Subtractor Circuit is assumed to operate linearly, disregarding non-linear effects within the specified operational range of the operational amplifier.

**2.3 Experiment procedure**

**Adder**

1.Connections were made as per the circuit diagram.

2. Input voltages were applied as follows:

(a) V1 = 5 V and V2 = 2 V

(b) V1 = 5 V and V2 = 5 V

(c) V1 = 5 V and V2 = 7 V

3. Using multimeter, the dc output voltage were measured at the output terminal.

4. For different values of V1 and V2, the output voltages were measured

**Subtractor**

1.Connections were made as per the circuit diagram.

2. The input voltages were applied as follows:

(a) V1 = 5 V and V2 = 2 V

(b) V1 = 5 V and V2 = 5 V

(c) V1 = 5 V, and V2 = 7 V

3. Using multimeter, the dc output voltage were measured at the output terminal.

4. For different values of V1 and V2,the output voltage were measured

**3. PRACTICAL IMPLEMENTATION**

**3.1 Set up of the circuit in prototyping**



***Figure 3 circuit diagram of adder and subtractor circuits***

**3.2 Data and measurement**

**Adder:**

|  |  |  |
| --- | --- | --- |
| V1(V) | V2(V) | V0(V) |
| 5V | 3V | -8V |
| 3V | 2V | -5V |

***Figure 4 table of results***

**Subtractor:**

|  |  |  |
| --- | --- | --- |
| V1(V) | V2(V) | V0(V) |
| 5V | 2V | -3V |
| 4V | 5V | 1V |

***Figure 5 table of results***

**4 RESULTS**

**Adder**

***figure 6 the output of the adder (summing amplifier) circuit using op amp***

**Subtractor**



***Figure 7 the output of the subtractor using an op amp***

**5 CONCLUSION AND RECOMMENDATION**

**5.1 Discussion**

**For the adder:**

1. Ideal Operational Amplifier (Op-Amp):

The operational amplifier is presumed to be ideal, possessing characteristics such as infinite open-loop gain, infinite input impedance, zero output impedance, and no offset voltage. While real Op-Amps have inherent limitations, assuming ideality simplifies the analysis for theoretical purposes.

2. Negligible Input Bias Current:

The input bias current of the operational amplifier is considered negligible. Although real Op-Amps exhibit some input bias current, for analytical purposes, it is deemed small enough not to significantly impact the circuit.

3. Zero Input Offset Voltage:

The operational amplifier's input offset voltage is set to zero in the assumptions. While practical Op-Amps may have minor offset voltages, this assumption streamlines the model for theoretical analysis.

4. Ideal Resistors:

Resistors within the circuit are treated as ideal, devoid of parasitic effects, temperature dependence, or manufacturing tolerances. While this simplification aids in calculations, it may not perfectly mirror the characteristics of real-world resistors.

5. Linear Operation:

The circuit is expected to operate in the linear region of the operational amplifier, where the output is directly proportional to the input. Non-linear effects are intentionally disregarded for the sake of theoretical analysis.

**For the Subtractor**:

1. Ideal Operational Amplifier (Op-Amp):

Similar to the Adder Circuit, the operational amplifier in the Subtractor Circuit is considered ideal to simplify the analysis.

2. Negligible Input Bias Current:

As in the Adder Circuit, the input bias current of the operational amplifier is assumed to be negligible.

3. Zero Input Offset Voltage:

The assumption of zero input offset voltage for the operational amplifier is maintained in the Subtractor Circuit.

4. Ideal Resistors:

Resistors within the circuit are assumed to be ideal, free from parasitic effects, temperature dependence, or manufacturing tolerances.

5. Linear Operation:

The Subtractor Circuit is assumed to operate linearly, neglecting non-linear effects within the specified operational range of the operational amplifier.

**5.2 conclusion**

**For the adder:**

1. Ideal Operational Amplifier (Op-Amp):

The operational amplifier is assumed to be ideal, possessing features such as infinite open-loop gain, infinite input impedance, zero output impedance, and no offset voltage. While real Op-Amps have inherent limitations, assuming ideality simplifies the analysis for theoretical purposes.

2. Negligible Input Bias Current:

The input bias current of the operational amplifier is considered negligible. Despite the existence of some input bias current in real Op-Amps, for analytical purposes, it is deemed sufficiently small not to significantly impact the circuit.

3. Zero Input Offset Voltage:

The operational amplifier's input offset voltage is assumed to be zero in these considerations. In practical scenarios, Op-Amps may exhibit minor offset voltages, but this assumption streamlines the model.

4. Ideal Resistors:

Resistors within the circuit are regarded as ideal, devoid of parasitic effects, temperature dependence, or manufacturing tolerances. While this simplifies calculations, it may not precisely reflect real-world resistor characteristics.

5. Linear Operation:

The circuit is expected to operate in the linear region of the operational amplifier, where the output is directly proportional to the input. Non-linear effects are deliberately excluded.

For the Subtractor:

1. Ideal Operational Amplifier (Op-Amp):

Similar to the Adder Circuit, the operational amplifier in the Subtractor Circuit is assumed to be ideal for the purpose of simplifying the analysis.

2. Negligible Input Bias Current:

As in the Adder Circuit, the input bias current of the operational amplifier is considered negligible.

3. Zero Input Offset Voltage:

The assumption of zero input offset voltage for the operational amplifier is upheld in the Subtractor Circuit.

4. Ideal Resistors:

Resistors within the circuit are assumed to be ideal, lacking parasitic effects, temperature dependence, or manufacturing tolerances.

5. Linear Operation:

The Subtractor Circuit is presumed to operate linearly, disregarding non-linear effects within the specified operational range of the operational amplifier.

**5.3 References**

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